Docket No.: 0756-7660

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)
Kiyoshi KATO et al.	)
Application No.: 10/573,527	) Art Unit: 2893
Filed: May 24, 2006	) Examiner: WOLDEGEORGIS, ERMIAS T
For: MEMORY DEVICE AND MANUFACTURING METHOD OF THE SAME	)

VERIFICATION OF TRANSLATION

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

I, Yoshimi Ando, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached English translation of the Japanese Patent Application Serial No. 2004-166274 filed on June 3, 2004; and

that to the best of my knowledge and belief the following is a true and correct English translation of the Japanese Patent Application Serial No. 2004-166274 filed on June 3, 2004.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 18th day of September, 2009

Yoshimi Ando

Name:: Yoshimi Ando

[Document Name] Patent Application

[Reference Number] P007930

[Filing Date] June 3, 2004

[Attention] Commissioner, Patent Office

[Inventor]

[Address] c/o Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi-shi, Kanagawa-ken

[Name] Kiyoshi KATO

[Inventor]

[Address] c/o Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi-shi, Kanagawa-ken

[Name] Tetsuji YAMAGUCHI

[Inventor]

[Address] c/o Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi-shi, Kanagawa-ken

[Name] Etsuko ASANO

[Inventor]

[Address] c/o Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi-shi, Kanagawa-ken

[Name] Konami IZUMI

[Patent Applicant]

[Identification Number] 000153878

[Name] Semiconductor Energy Laboratory Co., Ltd.

[Representative] Shunpei YAMAZAKI

[Indication of Handlings]

[Number of Prepayment Note] 002543

[Payment Amount] ¥16,000

[List of Attachment]

[Attachment] Scope of Patent Claims 1

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Name of Document] Scope of Patent Claims

[Claim 1]

A memory device comprising a memory cell which includes a semiconductor film having two impurity regions, a gate electrode, and two wirings connected to the respective impurity regions, over an insulating surface,

wherein the two wirings are insulated from each other since quality of the semiconductor film is altered by applying a voltage between the gate electrode and at least one of the two wirings in the memory cell.

[Claim 2]

A memory device comprising a first and a second memory cells each of which includes a semiconductor film having two impurity regions, a gate electrode, and two wirings connected to the respective impurity regions, over an insulating surface,

wherein the first memory cell has a state where the two wirings are insulated from each other since quality of the semiconductor film is altered by applying a voltage between the gate electrode and at least one of the two wiring, and

wherein the second memory cell has an initial state.

[Claim 3]

The memory device according to claim 1 or 2,

wherein one of, or two or more of the gate electrodes are provided.

[Claim 4]

A memory device comprising a memory cell which includes a semiconductor film having one or two impurity regions, an electrode, and two wirings connected to the respective impurity regions, over an insulating surface,

wherein the two wirings are insulated from each other since quality of the semiconductor film is altered by applying a voltage between the electrode and at least

one of the two wirings in the memory cell.

[Claim 5]

A memory device comprising a first and a second memory cells each of which includes a semiconductor film having one or two impurity regions, an electrode, and two wirings connected to the respective impurity regions, over an insulating surface,

wherein the first memory cell has a state where the two wirings are insulated from each other since quality of the semiconductor film is altered by applying a voltage between the electrode and at least one of the two wiring, and

wherein the second memory cell has an initial state.

[Claim 6]

The memory device according to claim 4 or 5,

wherein the electrode is interposed between the two wirings.

[Claim 7]

The memory device according to one of claims 4 to 6,

wherein one of, or two or more of the electrodes are provided.

[Document Name] Specification

[Title of the Invention] MEMORY DEVICE

[Technical Field]

[0001]

The present invention relates to a memory device, and more particularly to a nonvolatile memory device.

[Prior Art]

[0002]

In a society like modern society where many electronic appliances are used, various data is generated and used, and a memory device is required to store the data. Various memory devices produced and used today each have different advantages and disadvantages, and are selected to use depending on kinds of the data to be stored and used.

[0003]

For example, a volatile memory, in which its memory content is lost, when the power is turned off includes a DRAM and an SRAM. The volatile memory has strictly limited applications because of its volatility; however, it is used as a main memory device or a cache memory of a computer due to its short access time. As for a DRAM, the memory cell size is small, and therefore, its capacity can be increased easily; however, there are disadvantage that its control method is complex and the power consumption is high. Meanwhile, a memory cell of an SRAM is constituted by a CMOS and the manufacturing process and control method are easy; however, it is not suitable to increase its capacity since one memory cell needs six transistors.

[0004]

A nonvolatile memory, which holds its memory content even after the power is turned off, includes: a rewritable type, where the memory content can be rewritten many times; a write-once type, where the data can be written only once by the user; and a mask ROM, where the data content has been determined in producing the memory and the data content cannot be rewritten. As the rewritable type, there are an EPROM, a flash memory, a ferroelectric memory, and the like. As for the EPROM, although the writing operation is easy and unit cost per bit is relatively low, a dedicated program device and an eraser are required when writing and erasing. The flash memory and the

ferroelectric memory allow rewriting on a substrate in use, have a short access time, and consume low power; however, steps of fabricating a floating gate and a ferroelectric layer are required during the production, and the unit cost per bit is high.

[0005]

A memory cell of a write-once memory is constituted of a fuse, an antifuse, a cross pointer diode, an OLED (Organic Light Emitting Diode), a bistable liquid crystal element, or other devices whose state is changed by adding heat or light. In general, a memory device stores data since a memory cell selects one of the two states. The write-once memory device is produced with all memory cells having a first state, and only memory cells specified by a writing operation are changed to a second state. The change from the first state to the second state is irreversible and once the memory cell is changed, it cannot be restored.

[0006]

A write-once memory has a limit of temperature, materials, and the like in its manufacturing process, and is not manufactured on a silicon substrate in many cases. That is, the manufacturing process is completely different from a central processing unit (hereinafter referred to as a CPU), an arithmetic circuit, a rectification circuit, a control circuit, and the like (hereinafter these circuits are referred to as other functional circuits to be distinguished from a write-once memory), which are generally manufactured on a silicon substrate. For example, an antifuse write-once memory has a wiring, an antifuse layer, and a control element, which are manufactured over a plastic or metal substrate (see Patent Document 1). The memory device manufactured in this manufacturing method achieves low cost, large capacity, low power consumption, and a short access time. In the case of manufacturing one semiconductor device having a

certain function, however, a memory does not operate by itself and other functional circuits are necessarily required. Therefore, it is necessary to fabricate a memory such as a write-once memory and other functional circuits separately.

[0007]

On the other hand, an IC tag has been known today as an example of a semiconductor device where a memory and other functional circuits are fabricated on the same silicon substrate. Memories fabricated in an IC tag are an SRAM, a mask ROM, a flash memory, and a ferroelectric memory. In a mask ROM, the data content has been determined in manufacturing the memory, and it is not possible for an IC tag user to rewrite data. In addition, a piece of data is determined by one photomask; therefore, as many photomasks as kinds of data are required in the case of requiring a memory having a different data content. Thus, it is not practical for cost reasons.

[0008]

Note that a flash memory and a ferroelectric memory require additional steps for fabricating a memory such as a step for fabricating a floating gate and a ferroelectric layer in a gate insulating film. Meanwhile, all the circuits other than the memory formed in an IC tag can be fabricated in a range of CMOS manufacturing process.

[0009]

In recent years, technologies for manufacturing a thin film transistor (hereinafter referred to as a TFT) on an insulating substrate have been actively developed in order to manufacture display devices such as a liquid crystal display and an EL display. For example, not only a pixel portion of a display but also a driver circuit for displaying images on the display are manufactured on the same substrate by using TFTs. On an insulating substrate, the substrate is not capacitively coupled to a

wiring; thus, high speed operation of a circuit can be achieved. Accordingly, various functional circuits such as an arithmetic circuit and a memory device are proposed to be manufactured by using TFTs. Another advantage of manufacturing functional circuits on an insulating substrate is cost. A glass substrate and a plastic substrate are quite inexpensive as compared to a silicon substrate. Further, although a silicon substrate is limited to a small area, it is possible to use an insulating substrate with a larger area than a silicon substrate. Thus, the number of obtained products increases as compared to that of ones manufactured on a silicon substrate; as a result, it is possible to provide a quite inexpensive semiconductor device.

[0010]

Today, a memory device manufactured by using technologies for manufacturing a TFT includes a mask ROM, an SRAM, and a flash memory. An SRAM is formed of TFTs, and can be easily manufactured on the same substrate as other functional circuits; however, it has strictly limited applications because of its volatility. A mask ROM is not practical since photomasks are required to be changed for altering data. In the case of manufacturing a flash memory, steps for manufacturing a floating gate are required. Meanwhile, other functional circuits such as an arithmetic circuit manufacturing on an insulating substrate can be fabricated in a range of TFT manufacturing process.

[0011]

As set forth above, the present invention is made with the two technologies for its background: a technology related to manufacturing a memory device; and a technology for manufacturing a circuit over an insulating substrate such as a glass substrate or over an insulating surface.

[Patent Document 1] Japanese Patent Laid-Open No. 2003-36684

[Disclosure of the Invention]

[Problems to be Solved by the Invention]

[0012]

It is difficult to fabricate a nonvolatile memory circuit and other functional circuits on the same substrate according to conventional technologies; regardless of whether a substrate where a semiconductor integrated circuit is manufactured is a silicon substrate or an insulating substrate. However, if a memory and other functional circuits are manufactured separately to manufacture one device, they are required to be connected externally, which results in increasing a completed device size also. In addition, at least two or more circuits that are a memory and other functional circuits are manufactured; therefore, it is costly. Even if a memory and other functional circuits can be manufactured on the same substrate as a flash memory and a ferroelectric memory, steps required to fabricate the memory have to be added. In the manufacture of a semiconductor device, an increase in numbers of steps not only leads to high cost by itself, but also needs limiting product specifications, or decreases productivity.

[0013]

In other words, almost all memory devices conventionally manufactured require specific steps to manufacturing a memory device. Accordingly, there were problems that they cannot be manufactured on the same substrate as other functional circuits or that steps other than TFT manufacturing process need to be added even when they are manufactured on the same substrate as other functional circuits. This leads to extra cost for a memory in the manufacture of a semiconductor device having one function, for example, such as an IC tag.

[0014]

In view of the foregoing, the present invention has an objective to provide a manufacturing method of a write-once memory in a range of TFT manufacturing process similarly to other functional circuits manufactured on an insulating substrate. In addition, the present invention provides an easy-to-use, inexpensive memory device without limiting the product specifications and decreasing its productivity even when a memory is manufactured on the same substrate as other functional circuits.

[Means for Solving the Problems]

[0015]

In view of the foregoing problem, the present invention is characterized by a memory device having a write-once memory function by changing states such as quality alternation of a semiconductor film formed on an insulating substrate such as a glass substrate and a plastic substrate or a substrate having an insulated surface (hereinafter collectively referred to as an insulating substrate).

[0016]

According to one mode of the present invention, a memory device is characterized by including a memory cell which includes a semiconductor film having two impurity regions, a gate electrode, and two wirings connected to the above respective impurity regions, over an insulating surface. In the above memory cell, the above two wirings are insulated from each other since quality of the above semiconductor film is altered by applying a voltage between the above gate electrode and at least one of the above two wirings.

[0017]

According to another mode of the present invention, a memory device is

characterized by including a first and a second memory cells each of which includes a semiconductor film having two impurity regions, a gate electrode, and two wirings connected to the above respective impurity regions, over an insulating surface. The above first memory cell has a state where the above two wirings are insulated from each other since quality of the above semiconductor film is altered by applying a voltage between the above gate electrode and at least one of the above two wiring, and the second memory cell has an initial state. A binary value state of the insulating state or the initial state can be achieved.

[0018]

According to another mode of the present invention, a memory device is characterized by including a memory cell which includes a semiconductor film having one or two impurity regions, an electrode, and two wirings connected to the above respective impurity regions, over an insulating surface. In the above memory cell, the above two wirings are insulated from each other since quality of the above semiconductor film is altered by applying a voltage between the above electrode and at least one of the above two wirings.

[0019]

According to another mode of the present invention, a memory device is characterized by including a first and a second memory cells each of which includes a semiconductor film having one or two impurity regions, an electrode, and two wirings connected to the above respective impurity regions, over an insulating surface. The above first memory cell has a state where the above two wirings are insulated from each other since quality of the above semiconductor film is altered by applying a voltage between the above electrode and at least one of the above two wiring, and the above

second memory cell has an initial state. At this time, when seen from the top of the insulating substrate, the above electrode is interposed between the above two wirings.

[0020]

In the present invention, one of, or two or more of gate electrodes or electrodes may be included.

[Effect of the Invention]

[0021]

By using the aforementioned means, a write-once memory can be manufactured on an insulating substrate in a range of TFT manufacturing process. That is, the memory device of the present invention can be manufactured by TFT manufacturing process similarly to other functional circuits manufactured on an insulating substrate, which can suppress an increase in extra cost due to additional steps for a memory. Further, since a memory and other functional circuits can be manufactured by the same steps, the product specifications are not limited, and the productivity is not decreased either by manufacturing the memory.

[0022]

In addition, a glass substrate and a plastic substrate are quite more inexpensive than a silicon substrate. Further, although a silicon wafer is limited to a small-sized substrate, it is possible to use an insulating substrate with a larger area than a silicon substrate. Thus, the number of obtained products increases as compared to a silicon substrate, and it is possible to provide a quite inexpensive semiconductor device.

[0023]

According to the present invention, a write-once memory is manufactured in a range of TFT manufacturing process, and an easy-to-use, inexpensive memory device

can be provided without limiting the product specifications and with keeping high productivity even when a memory is manufactured on the same substrate as other functional circuits.

[Best Mode for Carrying Out the Invention]

[0024]

Embodiment modes of the present invention will be described below with reference to the drawings. However, it is to be easily understood for those skilled in the art that the present invention can be carried out according to many different embodiments, and that the embodiments or the details can be variously modified unless it departs from the content and the scope of the present invention. Therefore, the present invention should not be construed as being limited to the description of the embodiment modes. Note that in all the drawings, the same components or components having the similar function are denoted by the same reference numerals, and a repetitive description thereof is omitted.

[0025]

(Embodiment Mode 1)

When a voltage higher than required for normal operation of a TFT is applied between a gate electrode and at least one of two impurity regions (including a high concentration impurity region) of the TFT manufactured on an insulating substrate, a channel region of the TFT is insulated. In order to illustrate this operation, cross sectional views before and after applying a voltage to a TFT are shown as FIGS. 1(A) and (B) respectively. For example, a TFT 100 shown in FIG. 1(A) has a semiconductor film 102 on an insulating substrate 101, a gate insulating film 105 on the semiconductor film 102, and a gate electrode 106 thereon. The semiconductor film

102 includes two high concentration impurity regions 103 and a channel region 104. A TFT 107 in FIG. 1(B) schematically illustrates a TFT after applying a voltage. In the TFT 107, quality of the channel region 104 of the semiconductor film is altered at least and an insulated region 108 is formed under the gate electrode. Then, three terminals of the gate electrode and the two high concentration impurity regions 103 are insulated from each other. The insulated region 108 shown in FIG. 1(B) is schematically illustrated, and an actually-insulated region has various shapes.

[0026]

For example, in a TFT manufactured on a glass substrate, which has a channel length (hereinafter referred to as L) of 4 μm, a channel width (hereinafter referred to as W) of 4 μm, and a gate insulating film with a thickness (hereinafter referred to as GI) of 20 nm, a voltage of 25 V is applied between the gate electrode and at least one of the two high concentration impurity regions for 500 μseconds. Then, the channel region of the TFT is insulated and three terminals of the gate electrode and the two high concentration impurity regions are insulated from each other. Actual photographs before and after applying a voltage are shown in FIG. 10. FIG. 10(A) is the TFT before applying a voltage and FIG. 10(B) is the TFT after applying a voltage, which is seen from the back side of the glass substrate.

[0027]

Quality alteration in this specification of the present invention means specifically a change of at least the channel region into an insulating state, as shown in FIG. 10(A) to FIG. 10(B), due to applying a voltage to the TFT. It is needless to say that by changing the voltage application conditions, at least a channel region can be insulated even when the TFT has a different size from that shown here.

[0028]

In this manner, when a voltage higher than required for operation of a TFT is applied between a gate electrode and at least one of two impurity regions (high concentration impurity regions in this embodiment mode), a current flows through a gate insulating film. The insulating film is made of a highly resistant substance; therefore, heat is generated when a current flows therethrough. When a large amount of heat is generated in a TFT manufactured on an insulating substrate, there is no area where the heat can escape because an insulating substrate generally has low thermal conductivity. Therefore, the gate insulating film or a semiconductor film are burned by the heat. As a result, three terminals of the gate electrode and the two high concentration impurity regions can be insulated from each other. On the other hand, it can be considered that in a transistor on a silicon substrate, which has high thermal conductivity, heat generated when a current flows through a gate insulating film does not burn the insulating film and the silicon substrate.

[0029]

According to the experiment related to the present invention, when a voltage is applied between a gate electrode and at least one of two high concentration impurity regions, a channel region is insulated around 97% of the time. Then, it is confirmed that three terminals of the gate electrode and the two high concentration impurity regions are insulated from each other, namely they are altered into a non-conductive state. The rest of around 3% are defective-mode elements, where a channel region functions as a resistor after applying a voltage and the three terminals are in a conductive state. Defective-mode elements may be caused by dust in a semiconductor film or an insulating film. Therefore, improved manufacturing accuracy of TFTs

allows defective-mode elements to be further reduced. Alternatively, the elements in a defective mode can also be managed by making a gate electrode of a TFT to be a double gate or by providing a redundant circuit additionally.

[0030]

A memory device is a device which stores data when a memory cell selects one of two states. A memory device of the present invention can store data when a TFT as a memory cell selects one of two states: whether a channel region of the TFT remains in an initial state or is changed to an insulating state. In the present invention, by using the above structure, for example, a TFT in the initial state before applying a voltage is called a state "1," while the TFT including a channel region altered to an insulating state by applying a voltage is called a state "0," and then, a write-once memory is manufactured. This relation between the states of the TFT and the reference numerals "0" and "1" is not limited to this; however, the above relation is used in this specification of the present invention for convenience.

[0031]

A circuit diagram of a four-bit memory cell array is shown in FIG. 2 as a schematic view of the memory device of the present invention. The memory cell array includes two word lines 201, two bit lines 202, two source lines 204, and four TFTs 203. The word lines, the bit lines, and the source lines are denoted as numbers of W0, W1, B0, B1, S0, and Sl respectively as shown in the drawing. In the TFTs 203, a TFT selected by W0, B0, and S0 is denoted as 00; a TFT selected by W0, B1, and S0, 01; a TFT selected by W1, B0, and S0, 10; and a TFT selected by W1, B1, and S0, 11. As for these TFTs 203, when a voltage of 25 V or higher is applied between a gate electrode and at least one of two impurity regions of the TFTs for 500 μseconds, as set

forth above, channel regions of the TFTs are insulated.

[0032]

Described first is an example of a circuit operation for writing "0" to the TFT 00. The writing operation can be performed by applying a voltage between the gate electrode and at least one of the two impurity regions of the TFT 00. For example, a voltage of 25 V is applied to W0 and 0 V is applied to B0 and S0 for 500 μseconds. At this time, it is necessary to determine the voltages of W1, B1 and S1 so that "0" is not written to the other TFTs. For example, 0 V is applied to W1 and 10 V is applied to B1 and S1. By applying the above voltages, a voltage of 25 V is applied between the gate electrode and at least one of the two impurity regions of the TFT 00, thereby the channel region can be insulated.

[0033]

Brief description is made on the operation of the other TFTs while the operation of writing "0" to the TFT 00. First, since 25 V is applied to W0 and 10 V is applied to B1 and S1 in the TFT 01, a voltage between the gate electrode and at least one of the two impurity regions is 15 V. However, "0" is not written to the TFT 01 because a voltage of 25 V or higher is not applied thereto. Similarly, "0" is not written to the TFT 10 because 0 V is applied to W1, and 0 V is applied to B0 and S0. In the TFT 11, 0 V is applied to W1, and 10 V is applied to B0 and S0; therefore, a voltage of 10 V is applied between the gate electrode and the semiconductor film; however, "0" is not written thereto. Note that the voltages applied here are just examples, and a writing operation can be performed only to a selected TFT by appropriately determining voltages of each of the word lines 201, the bit lines 202, and the source lines 204.

[0034]

Described next is an example of a circuit operation for writing “1” to the TFT 00. When “1” is written to the TFT 00, no voltage is applied between the gate electrode and at least one of the impurity regions, and the TFT is maintained in an initial state. Accordingly, for example, all the word lines 201, the bit lines 202, and the source lines 204 may have the same voltage so that the operation of writing “0” is not to be performed. This is just an example and the potential of each of the word lines 201, the bit lines 202, and the source lines 204 may be determined appropriately by a controlling method of a circuit.

[0035]

An example of reading operation of the TFT 00 is described next. The reading operation may determine whether the TFT 00 remains in the state “1,” namely in the initial state without being subjected to the writing operation or the channel region of the TFT 00 is altered (changed) to the state “0,” namely to an insulating state by being subjected to the writing operation. Thus, a voltage of a threshold of the TFT 00 or higher is applied to the gate electrode of the TFT 00 to determine whether or not a current flows between the two high concentration impurity regions. First, before reading operation, B0 is precharged to 5 V. Then, 5 V is applied to W0, and 0 V is applied to S0 to set for reading the potential of B0. At this time, it is necessary to determine the voltages of W1, B1, and S1 so that the other TFTs are not selected. For example, 0 V is applied to W1 and S1 so that B1 is not to be selected to read. If the TFT 00 is not subjected to writing operation and is in the state “1,” the two impurity regions are conducted and B0 has a value which adds a threshold voltage of the TFT 00 to 0 V, since a voltage of 5 V is applied to W0. Meanwhile, if the TFT 00 is subjected to writing operation and is in the state “0,” B0 is maintained at a precharged voltage of 5

V since B0 and S0 are insulated from each other. The reading of the TFT 00 can thus be performed by applying a voltage equal to or higher than a threshold voltage to W0 and reading a change in the potential of B0.

[0036]

Brief description is made on the operation of the other TFTs while the reading operation of this TFT 00. First, since B1 is not selected to read, the reading does not involve the TFT 01 and the TFT 11. The TFT 10 does not change the potential of the bit line since W0 has 0 V. Therefore, the other TFTs do not influence the TFT 00 in its reading.

[0037]

As set forth above, in this embodiment mode, a memory cell has a binary value state: "a switching element" and "an insulator." Thus, a memory cell can be formed of only one TFT. This is an advantageous point that an area of a memory cell array can be reduced and memory capacity can be increased as well.

[0038]

(Embodiment Mode 2)

In a memory device of the present invention, a high concentration impurity may be added over the entire surface of a semiconductor film of a TFT serving as a memory cell. Instead, an impurity may be added to any portion of a semiconductor film and two wirings may be connected thereto; however, when forming an impurity region arbitrarily, the element does not function as a transistor. Meanwhile, if a structure where a high concentration impurity is added over the entire surface of a semiconductor film is employed, all the three terminals can be insulated from each other by applying a voltage between an electrode and at least one of two wirings.

[0039]

Described in this embodiment mode is an example where one impurity region (a high concentration impurity region in this embodiment mode) is manufactured in a semiconductor film on an insulating substrate and two wirings are connected to the above semiconductor film with one electrode interposed therebetween. In FIG. 3, top plan views and cross sectional views of an element in this case are illustrated. FIG. 3(A) is the same shape as that of a normal TFT in the case where a high concentration impurity is added to a semiconductor film before forming a gate electrode on an insulating film. FIG. 3(B) is a case where a gap with an appropriate width is formed in a gate electrode, and a high concentration impurity is added to a semiconductor film after forming the electrode. The gap should be positioned so nearly as the two wirings are insulated from each other when applying a voltage between the electrode and the semiconductor film. In both the elements of FIGS. 3(A) and (B),the two wirings is conducted through the high concentration impurity region of the semiconductor film; thus, these elements are referred to as "resistor elements" in this specification to be distinguished from TFTs.

[0040]

In FIGS. 3(A) and (B), each of the resistor elements includes a semiconductor film 301 on an insulating substrate 303, an insulating film 305 on the above semiconductor film 301, and an electrode 302 on the above insulating film 305. Two wirings 306 are connected to a high concentration impurity region 304 in the semiconductor film. The position of the high concentration impurity region in the semiconductor film and the positions of the wirings connected to the semiconductor film may be determined anywhere as long as the electrode 302 is interposed between

the two wirings. Additionally, also the shape of the electrode can be determined arbitrarily as in the case of FIG. 3(B) where the gap with an appropriate width is formed in the gate electrode. Further, the shape of the resistor element can be arbitrarily determined, and ones shown in FIG. 3 are just examples.

[0041]

For example, in the resistor element shown in FIG. 3(A), a voltage of 25 V is applied between the electrode and at least one of the two wirings of the resistor element having: L = 4 μm, W = 4 μm, and GI = 20 nm for 500 μseconds similarly to an example shown in Embodiment Mode 1. Then, all of three terminals of the electrode and the two wirings are insulated from each other. Needless to say, even if the element has a different size from that shown here, the three terminals can be insulated from each other by changing the voltage application conditions. In this embodiment mode, a write-once memory is manufactured by using such a structure.

[0042]

A circuit diagram of a four-bit memory cell array is shown in FIG. 4 as a schematic view showing this embodiment mode. The memory cell array includes two word lines 31, two bit lines 32, two selection control lines 33, four resistor elements 34, and four selection transistors 35. The word lines 31, the bit lines 32, and the selection control lines 33 are denoted as W0, W1, B0, B1, W'0, and W'1 respectively. A memory cell selected by W0 and B0 is 00, a memory cell selected by W0 and B1 is 01, a memory cell selected by W1 and B0 is 10, and a memory cell selected by W1 and B1 is 11. Similarly to the example shown in this embodiment mode, an electrode and two impurity regions are insulated from each other in the resistor element 34 by applying a voltage of 25 V or higher between the electrode and the impurity regions for 500

μseconds. Note that in this embodiment mode, the impurity region is sometimes formed in the entire surface of the semiconductor film; thus, it is described that a voltage is applied between the electrode and the semiconductor film.

[0043]

Described first is an example of a circuit operation for writing "0" to the memory cell 00. The writing operation can be performed by applying a voltage between the electrode and the semiconductor film, namely at least one of the two wirings connected to the semiconductor film of the resistor element in 00. For example, a voltage of 25 V is applied to W0 and 0 V is applied to B0 and W'0 for 500 μseconds. At this time, it is necessary to determine the voltages of W1, B1 and W'1 so that "0" is not written to the other resistor elements. For example, 0 V is applied to W1 and W'1 and 10 V is applied to B1. By applying the above voltages, a voltage of 25 V is applied between the electrode and the semiconductor film of the resistor element in 00, thereby three terminals of the electrode and the two wirings can be insulated from each other. The applied voltages shown here are just examples and the writing can be performed by other conditions as well.

[0044]

Brief description is made on the operation of the other memory cells in writing "0" to this memory cell 00. First, in the memory cell 01, since 25 V is applied to W0, 10 V is applied to B1, and 0 V is applied to W', a voltage between the electrode and the semiconductor film is 15 V. However, "0" is not written because a voltage of 25 V or higher is not applied thereto. As for the memory cell 10, "0" is not written since 0 V is applied to W1, W'1 and B0. As for the memory cell 11, 0 V is applied to W1 and W' and 10 V is applied to B0; therefore, a voltage of 10 V is applied between the electrode

and the semiconductor film; however, "0" is not written thereto. In this manner, the writing operation of "0" can be performed only to a selected memory cell by appropriately determining the voltages of the word lines 31, the bit lines 32, and the selection control lines 34.

[0045]

Described next is an example of a circuit operation for writing "1" to the memory cell 00. When "1" is written to the memory cell 00, no voltage is applied between the electrode and the semiconductor film of the resistor element, and an initial state is maintained. Accordingly, for example, all the word lines 31, bit lines 32, and selection control lines 33 may have the same voltage such as 0 V so that the writing operation of "0" is not performed. This is just an example and the potential of each of the word lines 31, the bit lines 32, and the selection control lines 33 may be determined appropriately by a controlling method of a circuit.

[0046]

An example of reading operation of the memory cell 22 is described next. The reading operation may determine whether the resistor element in the memory cell 00 remains a resistor element in the state "1," namely remains in the initial state without being subjected to the writing operation or the resistor element in the memory cell 00 is altered (changed) to the state "0," namely to an insulating state by being subjected to the writing operation. Thus, a voltage of a threshold or higher is applied to the gate electrode of the selection transistor in the memory cell 00 to determine whether B0 is conducted to one ground between the two high concentration impurity regions of the selection transistor. First, before reading operation, B0 is precharged to 5 V. Then, 5 V is applied to W'0. At this time, it is necessary to determine the voltages of W'1 and

B1 so that the other transistors are not selected. W0 and W1 are used only for writing and are not required in the reading operation. For example, 0 V is applied to W'1 so that B1 is not to be selected to read. If the resistor element in the memory cell 00 is not subjected to writing operation and is in the state "1," namely in the initial state, B0 is conducted to the ground and B0 has a value which adds a threshold voltage of the selection transistor to 0 V. Meanwhile, if the resistor element in the memory cell 00 is subjected to writing operation and is in the state "0," namely in the insulating state, B0 is maintained at a precharged voltage of 5 V even when 5 V is applied to W0 since B0 is insulated from the ground. The reading of the memory cell 00 can thus be performed by applying a voltage to W' and reading a change in the potential of B0.

[0047]

Brief description is made on the operation of the other memory cells in the reading operation of this memory cell 00. First, since B1 is not selected to read, the reading operation does not involve the memory cell 01 and the memory cell 11. The memory cell 10 does not change the potential of the bit line since W'0 has 0 V and the selection transistor does not operate. Therefore, the other memory cells do not influence the memory cell 00 in its reading.

[0048]

In this embodiment mode, a number of the elements in each memory cell is two, which increases the area of the memory cell array. However, a case of using a high voltage in writing (e.g., a decoder connected to W0 or W1) and a case of using a low voltage in reading (e.g., a decoder connected to W'0 or W'1) can be separated. In the case of using a high voltage, an L of a TFT is required to be large so that the TFT can withstand a high voltage. However, a large L is not suitable for high speed

operation; thus, an L is generally small in a system using a low voltage. Accordingly, it is very advantageous that these cases are separated in order to achieve high-speed operation and to facilitate operation control. Additionally, in this embodiment mode, TFTs can be used instead of the resistor elements 34 and a memory TFT and a selection TFT can be manufactured separately in a memory cell.

[Embodiment]

[0049]

(Embodiment 1)

In this embodiment, a manufacturing method of a TFT on a glass substrate is specifically described with reference to FIG. 5, FIG. 6 and FIG. 7. Description is made here with showing cross sectional structures of an n-type TFT and a p-type TFT.

[0050]

First, a peeling layer 501 is formed over a substrate 500 (FIG. 5(A)). An a-Si film (an amorphous silicon film) with a thickness of 50 nm is formed over a glass substrate (e.g., a 1737 substrate, product of Corning Incorporated) by low pressure CVD method. Note that as for the substrate, a quartz substrate, a substrate formed of an insulating material such as alumina, a silicon wafer substrate, a plastic substrate having enough heat resistance to the treatment temperature in the subsequent step, and the like can be employed as well as the glass substrate. In addition, as the peeling layer, it is preferable to use a film mainly containing silicon such as polycrystalline silicon, single crystalline silicon, and SAS (semi-amorphous silicon that is also referred to as microcrystalline silicon) as well as amorphous silicon; however, it is not limited to them. The peeling layer may be formed by plasma CVD method, sputtering, or the like as well as low pressure CVD method. Additionally, a film doped with an impurity such as

phosphorus may be employed as well. In addition, the thickness of the peeling layer is desirably 50 ~ 60 nm. It may be 30 ~ 50 nm in the case of employing an SAS.

[0051]

Next, a protective film 502 (also referred to as a base film or a base insulating film) is formed over the peeling layer 501 (FIG. 5(A)). Although a three-layer structure where a SiON film with a thickness of 100 nm\SiNO film with a thickness of 50 nm\a SiON film with a thickness of 100 nm are stacked is employed here , the material, the thickness, and the number of stacked layers are not limited to them. For example, instead of the SiON film as the bottom layer, a heat resistant resin such as siloxane with a thickness of 0.5 ~ 3 μm may be formed by spin coating method, slit coating method, droplet discharging method, or the like. Alternatively, a silicon nitride film (SiN, Si_3N_4, or the like) may be employed. Additionally, the thickness of each layer is preferably 0.05 ~ 3 μm and can be freely selected within the range. A silicon oxide film can be formed here by a method such as thermal CVD, plasma CVD, atmospheric pressure CVD, or bias ECRCVD using a mixed gas of SiH_4/O_2, TEOS (tetraethoxy silane)/O_2, or the like. In addition, a silicon nitride film can be typically formed by plasma CVD using a mixed gas of SiH_4/NH_3. Additionally, a SiON film or a SiNO film can be typically formed by plasma CVD using a mixed gas of SiH_4/N_2O.

[0052]

Next, TFTs are formed over the protective film 502. Note that thin film active elements such as organic TFTs and thin film diodes may be formed as well as the TFTs. First, as a TFT manufacturing method, an island shape semiconductor film 503 is formed on the protective film 502 (FIG. 5(B)). The island shape semiconductor film 503 is formed using an amorphous semiconductor, a crystalline semiconductor, or a

semi-amorphous semiconductor. A semiconductor film which mainly contains silicon, silicon germanium (SiGe), or the like can be employed. Note that in the case where a material mainly containing silicon such as a-Si is employed as the peeling layer 501 and the island shape semiconductor film 503, SiOxNy may be employed as the protective film 502 that is in contact with them from the point of view of ensuring the adhesiveness. Amorphous silicon with a thickness of 70 nm is formed here, and further, the surface thereof is treated with a solution containing nickel. Furthermore, a crystalline silicon semiconductor film is obtained by thermal crystallization process performed at a temperature of 500 ~ 750 °C, and the crystallinity may be improved by laser crystallization. In addition, plasma CVD method, sputtering method, LPCVD method, or the like may be employed as a film forming method. As a crystallization method, laser crystallization method, thermal crystallization method, or thermal crystallization using a catalyst other than nickel (Fe, Ru, Rh, Pd, Pd, Os, Ir, Pt, Cu, Au, or the like) may be performed, or they may be performed alternately a plurality of times.

[0053]

Alternatively, for the crystallization treatment of the semiconductor film having an amorphous structure, a continuous wave laser may be used, and in order to obtain a crystal with a large grain size during crystallization, a solid state laser capable of continuous wave may be used and it is preferable to apply a second harmonic, a third harmonic, and a fourth harmonic of a fundamental wave (the crystallization in the case of using this laser capable of continuous wave is referred to as CWLC). Typically, a second harmonic (532 nm) or a third harmonic (355 nm) of a Nd:YVO_4 laser (a fundamental wave: 1064 nm) may be applied. In the case where a continuous wave laser is used, laser light emitted from a continuous wave YVO_4 laser having an output of

10 W can be converted into a harmonic by a non-linear optical element. Alternatively, there is also a method for emitting a harmonic by putting a YVO_4 crystal or a $GdVO_4$ crystal and a non-linear optical element in a resonator. Then, the laser light is preferably formed in a rectangular shape or an ellipse shape at an irradiated surface with an optical system to irradiate a subject. In that case, an energy density of about 0.01 ~ 100 MW/cm^2 (preferably 0.1 ~ 10 MW/cm^2) is required. Then, the semiconductor film is irradiated while being moved relatively to the laser light at a speed of about 10 ~ 2000 cm/s.

[0054]

In addition, in the case where a pulsed laser is used, a frequency band of several tens Hz ~ several hundreds Hz is generally used; however, a pulsed laser having an extremely higher oscillation frequency of 10 MHz or higher may be used as well (the crystallization in the case of using a laser capable of pulsed oscillation having this frequency is referred to as MHzLC). It is said that it takes several tens nsec ~ several hundreds nsec to solidify a semiconductor film completely after the semiconductor film is irradiated with the pulsed laser light. By using the above high frequency band, it is possible to irradiate the next pulsed laser light after the semiconductor film is melted by laser light before it is solidified. Therefore, unlike the case of using the conventional pulsed laser, the solid-liquid interface can be moved continuously in the semiconductor film, and thus the semiconductor film having a crystal grain grown continuously in the scanning direction is formed. Specifically, it is possible to form an aggregation of crystal grains each of which has a width of 10 ~ 30 μm in the scanning direction of the contained crystal grain and a width of about 1 ~ 5 μm in the direction perpendicular to

the scanning direction. By forming such crystal grains of a single crystal extending long along the scanning direction, a semiconductor film having few crystal grain boundaries at least in the channel direction of the TFT can be formed. Note that in the case where the protective film 502 is partially formed using siloxane that is a heat resistant organic resin, heat leak from the semiconductor film can be prevented in the aforementioned crystallization, and crystallization can be performed effectively.

[0055]

The crystalline silicon semiconductor film is obtained through the aforementioned method. Note that the crystals are preferably aligned in the same direction as the source, channel and drain direction. In addition, the thickness of the crystalline layer is preferably 20 ~ 200 nm (typically 40 ~ 170 nm, and more preferably 50 ~ 150 nm). Subsequently, an amorphous silicon film for gettering of a metal catalyst was formed over the semiconductor film with an oxide film interposed therebetween, and gettering treatment was performed by heat treatment performed at a temperature of 500 ~ 750 °C. Furthermore, in order to control a threshold value as a TFT element, boron ions were injected into the crystalline silicon semiconductor film at a dosage on the order of $10^{13}/cm^2$. Then, etching was performed with a resist used as a mask to form the island shape semiconductor film 503. Note that the crystalline semiconductor film can be obtained by forming a polycrystalline semiconductor film directly by LPCVD (low pressure CVD) method using disilane (Si_2H_6) and germanium fluoride (GeF_4) as a source gas in forming a crystalline semiconductor film. Although the flow rate of the gas is Si_2H_6/GeF_4 = 20/0.9, the temperature for forming the film is 400 ~ 500 °C, and He or Ar is used as a carrier gas, it is not limited to them.

[0056]

Note that, preferably hydrogen or halogen of $1\times10^{19} \sim 1\times10^{22}$ cm^{-3}, and more preferably $1\times10^{19} \sim 5\times10^{20}$ cm^{-3} is added in a TFT, particularly in the channel region. In the case of using an SAS, $1\times10^{19} \sim 2\times10^{21}$ cm^{-3} is desirable. In either case, it is desirable that the amount of hydrogen or halogen be contained larger than that contained in single crystals used for an IC chip. According to this, if local cracks are generated at the TFT portion, it can be terminated by hydrogen or halogen.

[0057]

Next, a gate insulating film 504 is formed over the island shape semiconductor film 503 (FIG. 5(B)). The gate insulating film is preferably formed of a single layer or stacked layers of a film containing silicon nitride, silicon oxide, silicon nitride oxide, or silicon oxynitride by a thin film forming method such as plasma CVD method and sputtering method. In the case of stacking the layers, a three-layer structure of a silicon oxide film, a silicon nitride film, and a silicon oxide film from the substrate side is preferable, for example.

[0058]

Next, a gate electrode 505 is formed (FIG. 5(C)). Here, after Si and W (tungsten) are stacked and formed by sputtering method, etching is performed with a resist 506 used as a mask to form the gate electrode 505. Needless to say, the material, the structure, and the manufacturing method of the gate electrode 505 are not limited to this and can be selected appropriately. For example, a stacked structure of Si and NiSi (Nickel Silicide) doped with an n-type impurity, or a stacked structure of TaN (tantalum nitride) and W (tungsten) may be employed. Alternatively, it may be formed of a single layer by employing various kinds of conductive materials. In addition, a mask of SiOx or the like may be used instead of the resist mask. In this case, a patterning

forming step of the mask such as SiOx and SiON (such a mask made of an inorganic material is referred to as a hard mask) is added; however, the mask film is less reduced in etching as compared with the resist, thereby a gate electrode layer with a desired width can be formed. Alternatively, the gate electrode 505 may be selectively formed by droplet discharging method without using the resist 506. As the conductive materials, various kinds of materials can be selected depending on the function of the conductive film. Additionally, in the case where the gate electrode and an antenna are simultaneously formed, the material may be selected in consideration of their functions. Note that, as an etching gas for forming the gate electrode by etching, a mixed gas of CF_4, Cl_2, and O_2, or a Cl_2 gas was employed; however, it is not limited to this.

[0059]

Next, portions to be p-type TFTs 507 are covered with a resist 509. An impurity element 510, which imparts n-type (typically, P (phosphorous) or As (arsenic)) is doped to the island shape semiconductor films of n-type TFTs 508 at a low concentration with the gate electrode used as a mask (a first doping step, FIG. 5(D)). The first doping step is performed under such conditions as a dosage of 1×10^{13} ~ $6\times10^{13}/cm^2$ and an accelerated voltage of 50 ~ 70 keV; however, it is not limited to them. By this first doping step, doping through the gate insulating film 504, what is called, through doping is performed to form a couple of low concentration impurity regions 511. Note that the first doping step may be performed to the entire surface without covering the p-type TFT regions with the resist 509.

[0060]

Next, after the resist 509 is removed by ashing or the like, another resist 512 covering the n-type TFT regions is formed. An impurity element 513, which imparts

p-type, (typically, B (boron)) is doped to the island shape semiconductor films of the p-type TFTs 507 at a high concentration with the gate electrode used as a mask (a second doping step, FIG. 5(E)). The second doping step is performed under such conditions as a dosage of $1\times10^{16} \sim 3\times10^{16}/cm^2$ and an accelerated voltage of 20 ~ 40 keV. By this second doping step, through doping is performed through the gate insulating film 504 to form a couple of p-type high concentration impurity regions 514.

[0061]

Next, after the resist 512 is removed by ashing or the like, an insulating film 601 is formed over the surface of the substrate (FIG. 6(A)). A SiO_2 film with a thickness of 100 nm is formed here by plasma CVD method. Then, the entire surface of the substrate is covered with a resist 602, and the resist 602, the insulating film 601, and the gate insulating film 504 are etched and removed by etch back to form a sidewall 603 in a self-aligned manner (FIG. 6(B)). As an etching gas, a mixed gas of CHF_3 and He is employed. Note that if the insulating film is formed on the back side of the substrate as well during forming the insulating film 601, the insulating film on the back side is etched and removed with the resist 602 used as a mask (this is called a back side treatment).

[0062]

The forming method of the sidewall 76 is not limited to the aforementioned one. For example, methods shown in FIG. 7 can be employed. FIG. 7(A) shows the case where an insulating film 701 has a two or more layer stacked structure. As the insulating film 701, for example, a two-layer structure of a SiON (silicon oxynitride) film with a thickness of 100 nm and an LTO film (a low temperature oxide film) with a thickness of 200 nm. The SiON film is formed by plasma CVD method, and as the

LTO film, a SiO_2 film is formed by low pressure CVD method. Then, etch back is performed with the resist 44 used as a mask, thereby forming the sidewall 76 shaped by an L shape and an arc shape. In addition, FIG. 7(B) shows the case where etching is performed so that the insulating film 702 is left during the etch back. The insulating film 702 in this case may be a single layer structure or a stacked layer structure. The above sidewall serves as a mask when an n-type impurity is doped at a high concentration in the subsequent step to form a low concentration impurity region or a non-doped offset region under the sidewall 603. In any of the aforementioned forming methods of the sidewall, the conditions of the etch back may be changed appropriately depending on the width of the low concentration impurity region or the offset region which is desired to be formed.

[0063]

In addition, in the semiconductor device of the present invention, it is known that the memory cell operates without sidewalls. Therefore, the cases are shown as follows: a step where side walls are formed on the two TFTs on the left side in FIG. 6(B) and thereafter, and a step where side walls are not formed on the two TFTs on the right side in FIG. 6(B) and thereafter.

[0064]

Next, another resist 604 covering the p-type TFT regions is formed. An impurity element 605, which imparts n-type, (typically, P or As) is doped at a high concentration with the gate electrode 505 and the sidewall 603 used as masks (a third doping step, FIG. 6(C)). The third doping step is performed under such conditions as a dosage of $1\times10^{13} \sim 5\times10^{15}/cm^2$ and an accelerated voltage of $60 \sim 100$ keV. By this third doping step, a couple of n-type high concentration impurity regions 606 are

formed. Note that thermal activation of the impurity regions may be performed after the resist 604 is removed by ashing or the like. For example, after a SiON film with a thickness of 50 nm is formed, heat treatment may be performed at 550 °C for four hours in a nitrogen atmosphere. Alternatively, after a SiNx film containing hydrogen is formed to have a thickness of 100 nm, and heat treatment is performed at 410 °C for one hour in a nitrogen atmosphere; therefore, defects in the crystalline semiconductor film can be improved. This enables to, for example, terminate a dangling bond in the crystalline silicon and is called a hydrotreatment step. Furthermore, after that, a SiON film with a thickness of 600 nm is formed as a cap insulating film for protecting the TFT. Note that the hydrotreatment step may be performed after the formation of the SiON film. In this case, a SiNx\SiON film can be continuously formed. In this manner, the insulating film includes three layers of SiON\ SiNx\ SiON over the TFT; however, the structure and the materials are not limited to them. In addition, it is desirable that such insulating films are preferably formed, since they also have a function to protect the TFT.

[0065]

Next, an interlayer film 607 is formed over the TFT (FIG. 6(D)). As the interlayer film 607, a heat resistant organic resin such as polyimide, acrylic, polyamide, and siloxane can be employed. As the forming method, spin coating, dipping, spray application, droplet discharging method (inkjet method, screen printing, offset printing, or the like), a doctor knife, a roll coater, a curtain coater, a knife coater, or the like can be employed depending on the material thereof. Alternatively, an inorganic material may be employed, and silicon oxide, silicon nitride, silicon oxynitride, PSG (phosphosilicate glass), BPSG (boron phosphosilicate glass), an alumina film and the

like can be employed in such a case. Note that these insulating films may also be stacked to form the interlayer film 607. Furthermore, a protective film 608 may be formed over the interlayer film 607. As the protective film 608, a film containing carbon such as DLC (diamond like carbon) and carbon nitride (CN), a silicon oxide film, a silicon nitride film, a silicon nitride oxide film, or the like can be employed. As the forming method, plasma CVD method, atmospheric pressure plasma, or the like can be employed. Alternatively, a photosensitive or nonphotosensitive organic material such as polyimide, acrylic, polyamide, resist, or benzocyclobutene, or a heat resistant organic resin such as siloxane may be employed. Note that a filler may be mixed into the interlayer film 607 or the protective film 608 in order to prevent these films from being detached or cracked due to stress generated by a difference of thermal expansion coefficients between the interlayer film 607 or the protective film 608 and a conductive material or the like forming a wiring which is to be formed later.

[0066]

Next, after forming a resist, contact holes are formed by etching, and a wiring 609 is formed (FIG. 6(D)). As a gas used for etching when forming the contact holes, a mixed gas of CHF_3 and He was employed; however, it is not limited to this. Here, the wiring 609 has a five-layer structure of Ti\TiN\Al-Si\Ti\TiN, is formed by sputtering method, and is patterned then. Note that, by mixing Si into the Al layer, hillock can be prevented from generating in the resist baking when the wiring is patterned. In addition, instead of Si, Cu of about 0.5% may be mixed. Additionally, due to sandwiching the Al-Si layer between Ti and TiN, hillock resistance can be further improved. Note that it is desirable that the aforementioned hard mask formed of SiON or the like is employed in the patterning. Note that the material and the forming

method of the wirings are not limited to them, and the aforementioned material used for the gate electrode may be applied as well.

[0067]

Through the aforementioned steps, a semiconductor device having TFTs is completed. The semiconductor device includes an IC tag. Note that although a top gate structure is employed in this embodiment, a bottom gate structure (an inverted staggered structure) may be employed as well. Note that, over a region where a thin film active element portion such as a TFT does not exist, a base insulating film material, an interlayer insulating film material, and a wiring material are mainly provided. It is desirable that the region where a thin film active element portion does not exist occupies 50% or more, and preferably 70 ~ 95% of the whole semiconductor device. Meanwhile, it is preferable that an island shape semiconductor region (island) of the active element including the TFT portion occupies 1 ~ 30%, and more preferably 5 ~ 15% of the whole semiconductor device. In addition, as shown in FIG. 6(D), it is desirable that the thickness of the upper and lower protective layers or the interlayer film of the TFT in the semiconductor device is controlled so that the distance (t_{under}) from the semiconductor layer to the lower protective layer may be the same or substantially the same as the distance (t_{over}) from the semiconductor layer to the upper interlayer film (or the protective layer if a protective layer is formed). By disposing the semiconductor layer in the middle of the semiconductor device in this manner, stress applied to the semiconductor layer can be alleviated, thereby generation of cracks can be prevented.

[0068]

(Embodiment 2)

Described in this embodiment is an example of a semiconductor device incorporating the memory device of the present invention on the same substrate. An IC tag can be taken as an example of a semiconductor device where a memory and other functional circuits are manufactured on the same substrate. In FIG. 8(A), a block diagram of an IC tag is shown. An IC tag 801 includes an RF circuit 802, a power supply circuit 803, a command control circuit 804, a clock 805, a congestion control circuit 806, a memory control circuit 807, a memory 808, and an antenna 809. These functional circuits are manufactured on the same insulating substrate. Note that the antenna 809 may be manufactured on the same substrate. Alternatively, only a terminal conneting the antenna may be manufactured on the same substrate, and the antenna may be provided externally; thus, is surrounded by a dashed line in the drawing.

[0069]

In the IC tag 801, all the circuits except for the memory 808 can be manufactured in a range of the TFT manufacturing process. Here, the memory device of the present invention is incorporated in the memory 808, and all the circuits can be manufactured by the same process. In the case where the semiconductor device is formed on one substrate as in this embodiment, all the circuits can be manufactured by the same process, which leads to realizes improved productivity and cost saving.

[0070]

In addition, a write-once memory can serve its function sufficiently because the IC tag, similarly to a bar code, is not necessary to change the content afterward once the data content in the memory is determined first. For an IC tag whose objective is to be used for individual recognition and goods management, it can provide improved

security that data written once cannot be rewritten. Furthermore, the IC tag should hold data for a long period; therefore, a write-once memory to which data is written by an irreversible operation is suitable as a memory incorporated in the IC tag. In addition, if data should be written during the use of the IC tag, it is also possible that available memory is reserved as needed. In this manner, by incorporating the memory device of the present invention in the IC tag, high-security and easy-to-use product for users can be provided.

[0071]

Although an IC tag where semiconductor devices are manufactured on an insulating substrate is a device which operates only with the devices, the memory device of the present invention can also be used as a component of a device. The example is shown in FIG. 8(B). An electronic appliance 810 which is generally used at home, for example, a rice cooker, an air conditioner, or the like includes a CPU 812, a memory 811, an I/O controller 813, and an external device 814. The memory 811 incorporated in this electronic appliance is a program ROM where operating data of the appliance has been written before shipment thereof.

[0072]

The CPU 812, the memory 811, and the I/O controller 813 are presently manufactured as individual ICs; however, they can be manufactured on the same insulating substrate by using TFTs. It is largely advantageous that the circuits are manufactured on the same substrate even for a component of the appliance as in this embodiment. For example, the CPU 812, the memory 811, and the I/O controller 813 are presently manufactured as individual ICs; therefore, they are connected to each other with external wirings. Meanwhile, if they are manufactured on the same

substrate, wirings can be made in the substrate, and the size of the component is reduced. Additionally, steps and cost for connection are reduced, which results in cost saving of the product.

[0073]

In addition, since the operating data written to the memory is not required to be rewritten after shipment of the product, a write-once memory can serve its function sufficiently. Furthermore, the data can be written easily; therefore, the data content can be determined and written at the last stage of the manufacture of the product taking a change or update of the written data into consideration.

[0074]

(Embodiment 3)

Described in this embodiment are measures against writing defective-mode elements of a memory cell by using FIG. 9. In FIG. 9, top plan views and cross sectional views of a TFT are shown. A TFT includes a semiconductor film 901 on an insulating substrate 903, a gate insulating film 905 on the above semiconductor film 901, and a gate electrode 902 on the above gate insulating film 905. The semiconductor film 901 has high concentration impurity regions 904, and two wirings 906 are connected to the high concentration impurity regions respectively. In the memory cell in the memory device of the present invention, a defective mode 907 for a writing operation is generated in rare cases as shown in FIG. 9(A). When a voltage is applied between a gate electrode and a semiconductor film, three terminals of a TFT are generally insulated from each other; however, in a defective-mode element, the semiconductor film 901 and the gate insulating film 905 serve as a resistor and the three terminals are conducted to each other.

[0075]

As one measure for preventing this, it is suggested that two gate electrodes are provided over a TFT, and a double gate is adopted as shown in FIG. 9(B). A reason why defective-mode element is generated is supposed to be dust in a semiconductor film or an insulating film; therefore, the generation is at random. Even if the defective mode 907 is generated in one channel region of the double gate as shown in the drawing, for example, the two electrodes 906 are insulated between them as long as the other channel region becomes an insulating region 908. Therefore, the TFT can be used as a normal memory cell. Specifically, according to the present data, generation of a defective mode is about 3% of the time. Since the generation of a defective mode is generated at random, if a double gate is adopted, the generation can be probabilistically reduced to 0.1% or less.

[0076]

It is supposed that a defective-mode element is still generated with the increase in memory capacity of the memory. In such a case, a redundant circuit can be additionally provided similarly to a memory device produced today. Alternatively, by controlling an external circuit, access to an address of the defective-mode element can be prohibited as a flash memory.

[Brief Description of the Drawings]

[0077]

[FIG. 1] schematic views showing operations of a memory cell in a memory device of the present invention.

[FIG. 2] an example of a memory cell array.

[FIG. 3] top plan views and cross sectional views of a resistor element.

[FIG. 4] an example of a memory cell array.

[FIG. 5] diagrams showing an order of a TFT manufacturing process.

[FIG. 6] diagrams showing an order of a TFT manufacturing process.

[FIG. 7] diagrams showing an order of a TFT manufacturing process.

[FIG. 8] application examples of a memory device of the present invention.

[FIG. 9] examples of a memory cell in a memory device of the present invention.

[FIG. 10] photographs of TFTs of the present invention before and after a voltage is applied are shown.

[Document Title] Drawing

[FIG. 1]

[FIG. 2]

[FIG. 3]

[FIG. 4]

[FIG. 5]

[FIG. 6]

[FIG. 7]

[FIG. 8]

[FIG. 9]

[FIG. 10]

[Document Title] Abstract

[Problem]

It is an objective to provide an easy-to-use and inexpensive memory device for users without limiting specifications for the memory, and with improving productivity

even when a memory is manufactured on the same substrate as other functional circuits.

[Solving Means]

The memory device of the present invention is characterized by including a memory cell which includes a semiconductor film having two impurity regions, a gate electrode, and two wirings connected to the respective impurity regions, over an insulating surface. In the memory cell, the two wirings are insulated from each other since quality of the semiconductor film is altered by applying a voltage between the gate electrode and at least one of the two wirings.